#2
8-10-01

PATENTS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Louis L. Hsu et al.	**Examiner:**	Unassigned
Serial No:	09/827,073	**Art Unit:**	2185
Filed:	April 5, 2001	**Docket:**	YOR920000587US1 (13958)
For:	ULTRA HIGH-SPEED DDP-SRAM CACHE	**Dated:**	August 3, 2001

Assistant Commissioner for Patents
United States Patent and Trademark Office
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R. §§ 1.97 and 1.98, it is requested that the following reference, which is also listed on the attached Form PTO-1449, be made of record in the above-identified case.

1. "An 8ns Random Cycle Embedded RAM Macro with Dual-Port Interleaved DRAM Architecture (D^2RAM)", Yasuhiro Agata et al, 2000 IEEE International Solid-State Circuits Conference, 9 pages.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner of Patents and Trademarks, Washington, D.C. 20231 on August 3, 2001.

Dated: August 3, 2001

Janet Grossman
Janet Grossman

Applicants are submitting a copy of the above-cited reference.

Inasmuch as this Information Disclosure Statement is being submitted in accordance with the schedule set out in 37 C.F.R. § 1.97(b), no statement or fee is required.

Respectfully submitted,

William C. Roch
Registration No. 24,972

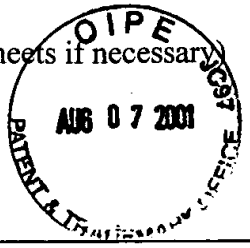
Scully, Scott, Murphy & Presser
400 Garden City Plaza
Garden City, New York 11530
(516) 742-4343

WCR/sf

Form PTO-1449 (REV. 7-80) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

LIST OF PRIOR ART CITED BY APPLICANT

(Use several sheets if necessary)



Atty. Docket No.	Serial No.
YOR920000587US1 (13958)	09/827,073

RECEIVED
AUG 0 9 2001
Technology Center 2100

Applicant	
Louis L. Hsu et al.	
Filing Date	**Group**
April 5, 2001	

U.S. PATENT DOCUMENTS

EXAMINER INITIAL*		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (if appropriate)
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO

OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

		"An 8ns Random Cycle Embedded RAM Macro with Dual-Port Interleaved DRAM Architecture (D^2RAM)", Yasuhiro Agata et al, 2000 IEEE International Solid-State Circuits Conference, 9 pages.

EXAMINER	DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.